

# DATA SHEET



## **PEMD6**

**NPN/PNP resistor-equipped  
transistors;**

**R1 = 4.7 k $\Omega$ , R2 = open**

Product specification  
Supersedes data of 2001 Oct 22

2001 Nov 07

**NPN/PNP resistor-equipped transistors;  
R1 = 4.7 kΩ, R2 = open**

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**FEATURES**

- 300 mW total power dissipation
- Very small 1.6 × 1.2 mm ultra thin package
- Self alignment during soldering due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

**APPLICATIONS**

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

**DESCRIPTION**

NPN/PNP resistor-equipped transistors in a SOT666 plastic package.

**MARKING**

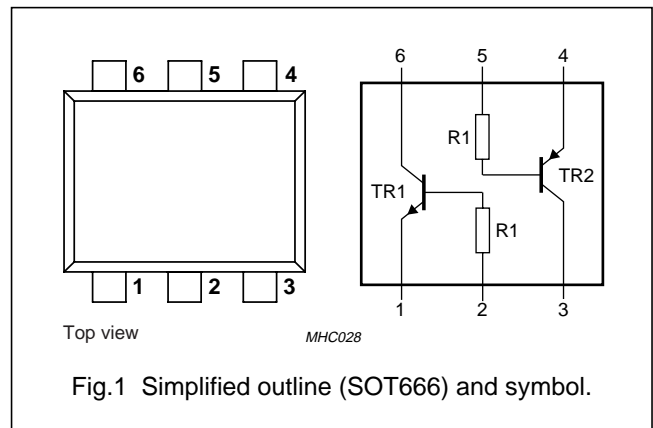
TYPE NUMBER	MARKING CODE
PEMD6	D6

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	50	V
I <sub>CM</sub>	peak collector current	100	mA
TR1	NPN	–	–
TR2	PNP	–	–
R1	bias resistor	4.7	kΩ
R2	open	–	–

**PINNING**

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CB0</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>i</sub>	input voltage TR1				
	positive		–	+40	V
	negative		–	–10	V
	input voltage TR2				
	positive		–	+10	V
	negative		–	–40	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

**Notes**

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

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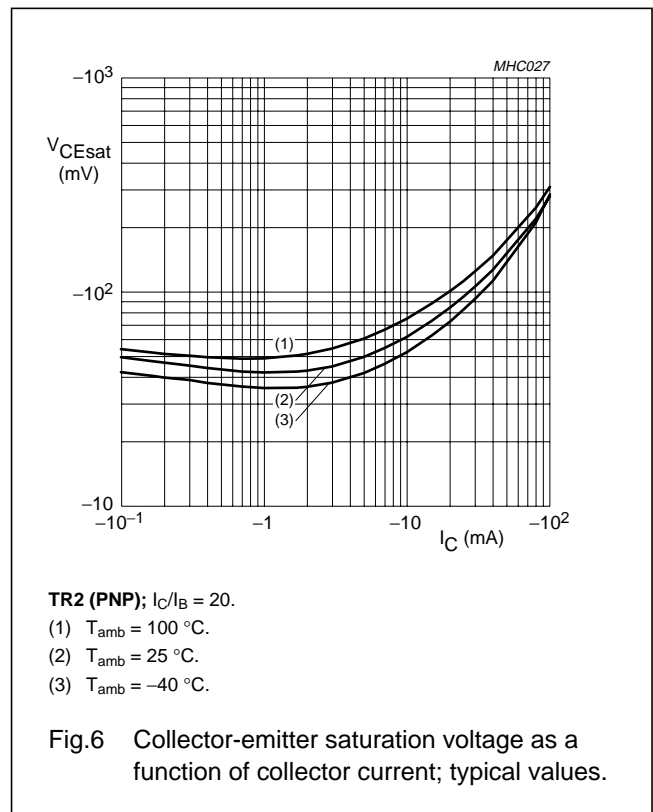
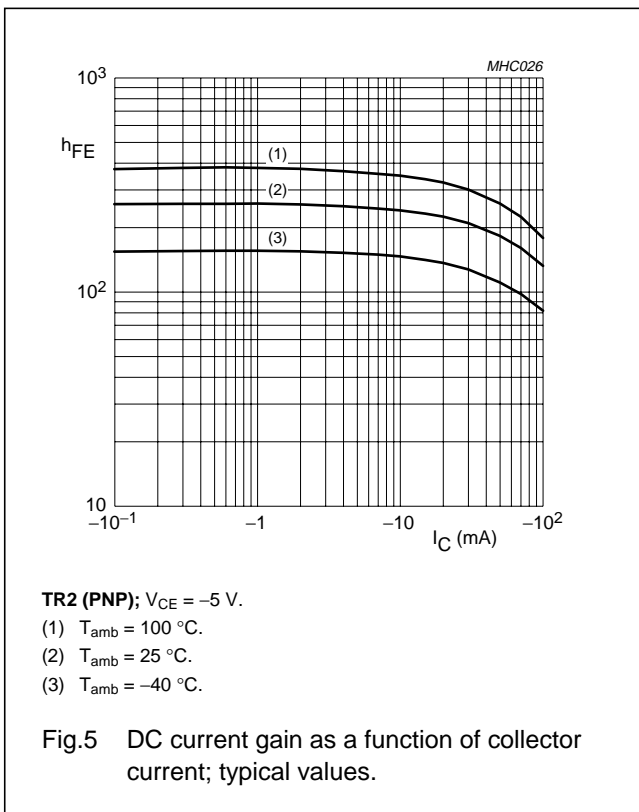
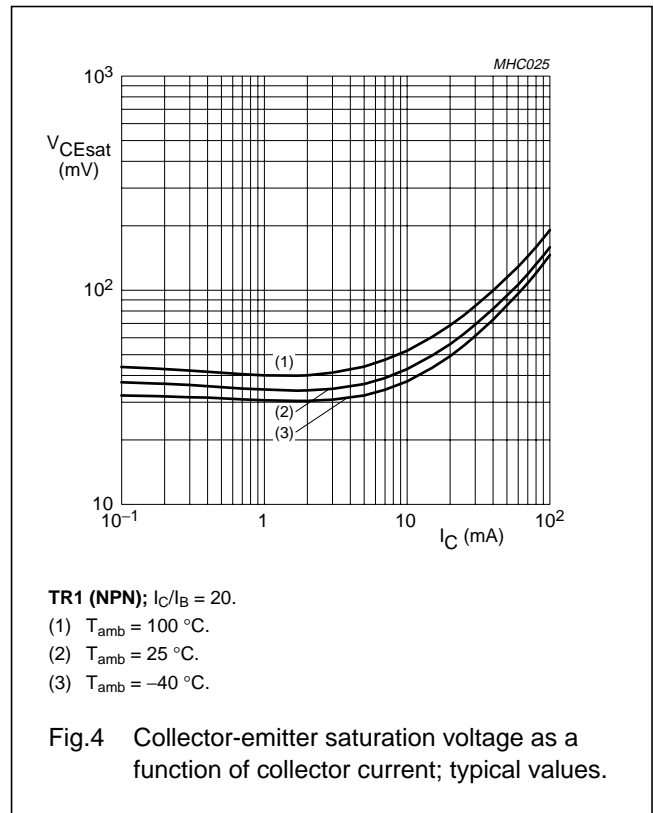
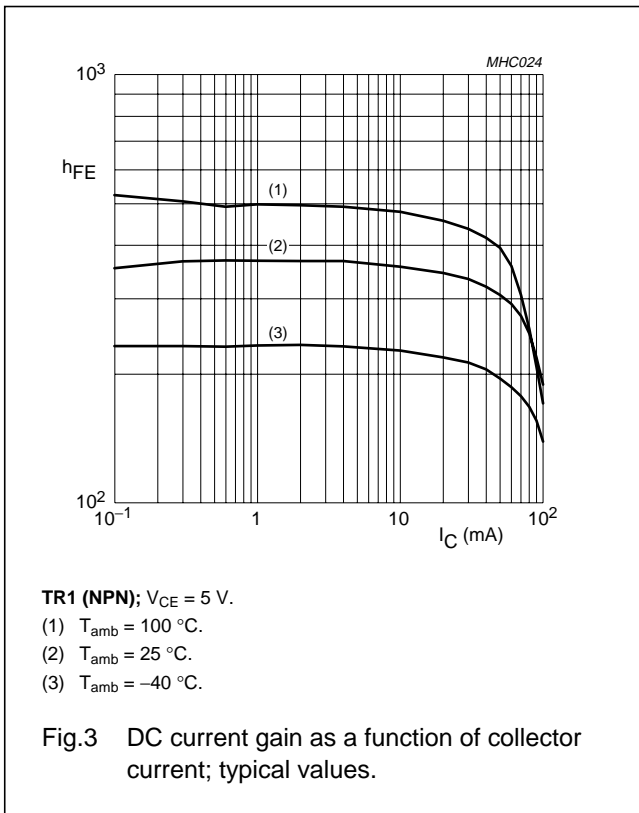
**CHARACTERISTICS**

T<sub>amb</sub> = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 50 V; I <sub>B</sub> = 0	–	–	1	$\mu$ A
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	–	–	50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	–	–	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 10 mA	200	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 5 mA; I <sub>B</sub> = 0.25 mA	–	–	100	mV
R1	input resistor		3.3	4.7	6.1	k $\Omega$
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)	–	–	3	pF	

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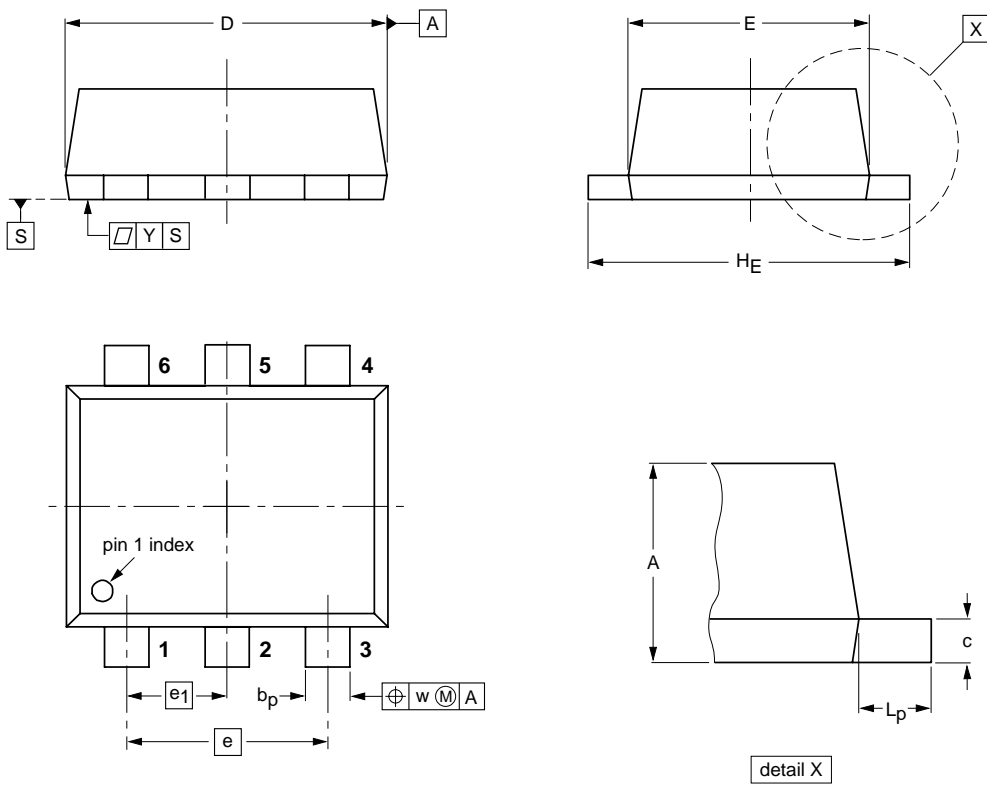
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						-01-01-04 01-08-27

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